AD-A174 580 DEVELOPMENT OF A PLANAR HETEROJUNCTION BIOPOLAR TRANSISTOR FOR VERY HIGH (U) CALIFORNIA UNIV SANTA BARBARA DEPT OF ELECTRICAL AND COMPUTER

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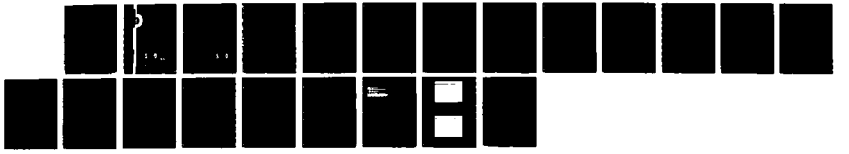

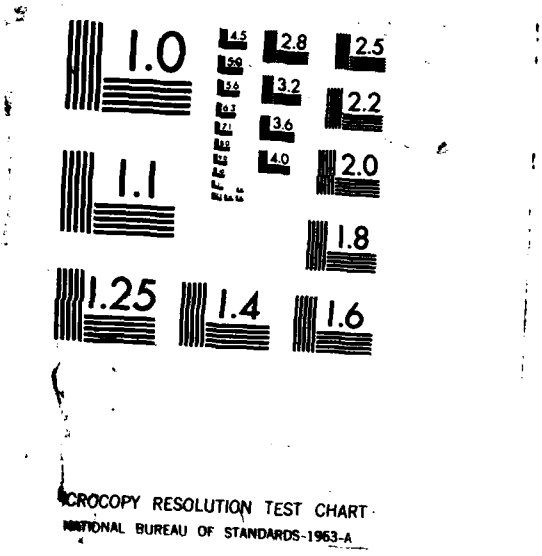
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Graded regions of n-(Ga,In)As and p-Ga(As,Sb) were incorporated side-by-side as emitter and base contacts respectively, into an npn (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). The process involved two separate MBE growths, leading to base contact regions that were self-aligned to the emitter mesas. The devices could be easily probed with pressure contacts even prior to any metallization, and excellent characteristics were obtained after final metallization. Contact resistivities of $5 \times 10^{-7}\ \Omega cm^2$ and $3 \times 10^{-6} \Omega cm^2$ were measured using the 4-point Kelvin technique for n and p-type graded-gap ohmic contact structures, respectively.

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1 Mar 86 - 29 Jun 86

Development of a Planar Heterojunction Bipolar Transistor for Very High Speed Logic

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Abstract

Graded regions of n-(Ga,In)As and p-Ga(As,Sb) were incorporated side-by-side as emitter and base contacts respectively, into an npn (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). The process involved two separate MBE growths, leading to base contact regions that were self-aligned to the emitter mesas. The devices could be easily probed with pressure contacts even prior to any metallization, and excellent characteristics were obtained after final metallization. Contact resistivities of $5 \times 10^{-7}\ \Omega cm^2$ and $3 \times 10^{-6} \Omega cm^2$ were measured using the 4-point Kelvin technique for n and p-type graded-gap ohmic contact structures, respectively.

Introduction

The following report presents a summary of the research results from the project "Development of a planar heterojunction bipolar transistor for very high speed logic" over the interval from 1 Mar 86 to 29 Jun 86. The work performed during the period 1 Oct 84 through 1 Mar 86 was presented in the Annual Technical Report #3 dated 28 Mar 1986. The following report therefore describes the progress during the interim.

In the previous reporting period a new direction toward improvement in performance and fabrication techniques for the AlGaAs/GaAs HBT was successfully established and was shown to be highly promising. Since the contacts to the device are highly critical in achieving the theoretical performance of the HBT, an alternative to the Au/Ge/Ni and AU/Zn "ohmic" contact systems was evaluated. This approach utilized a graded transition between n^+-AlGaAs and n^+-InAs for n-type contacts and p^+-GaSb for p-type contacts. It is well known that the Fermi level in n-InAs is pinned inside the InAs conduction band. Not as well known is the similar property for p-GaSb, that is the Fermi level is pinned in the valence band. Therefore, non-alloyed ohmic contacts will be possible on both material systems. Non-alloyed contacts are desireable because the alloying process caused penetration of the metal regions into the semiconductor. This penetration must be allowed for in the design of an emitter structure, for example, which forces the thickness to be larger than desireable for best performance. In addition, the nonalloyed contact will allow the same metal to

be used for both p and n-type contacts, opening up the possibility for self-aligned structures. An HBT device with graded-gap base and emitter contacts was grown by a selective regrowth technique, fabricated, and demonstrated to have a current gain of 20 when contacted only by tungsten wire probes (no metallization at all).

In the present reporting period, several more runs were made to fabricate AlGaAs/GaAs HBTs with non-alloyed contacts and devices having good I/V characteristics after final metallization were obtained. Both base and emitter metallizations were done in one step with Ti/Au, and no alloying was needed. The details of this work are given in a paper submitted to the IEEE Electron Device Letters, a preprint of which has been attached. The results were also presented at the Device Research Conference held at the University of Massachusetts at Amherst in June 1986.

The devices fabricated with the existing mask sets had rather large emitter sizes (the smallest being 20μm x 20μm) and were unsuitable for high frequency testing. The layout and fabrication of a new mask set that allows for fabrication of devices with narrow emitters (5μm x 20μm) has been completed. The devices are suitably configured for bonding onto substrates for high frequency measurements. First pass devices (with non-alloyed contacts), fabricated with the new mask sets showed dc current gains of 60. High frequency testing of these devices will be done as soon as we obtain an rf-test fixture.

Another feature of the new mask set is that it provides for making contact resistance measurements on the base and emitter contacts using the transmission

line method (TLM). Our initial measurements of the contact resitivities were made using the 4-point Kelvin method. The Kelvin technique is extremely sensitive to misalignment between the contact and the mesa, as has been recently shown in the literature, and might have led to unduly optimistic estimates of the contact resistivities. Preliminary measurements using the TLM method on the base and emitter mesas indicate resistivities of about $1 \times 10^{-6}\ \Omega cm^2$ for the n-type contacts and about $5 \times 10^{-6}\ \Omega cm^2$ for p-type contacts.

An (Al,Ga)As/GaAs heterostructure bipolar transistor with non-alloyed graded-gap ohmic contacts to the base and emitter

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Abstract

Graded regions of n-(Ga,In)As and p-Ga(As,Sb) were incorporated side-by-side as emitter and base contacts respectively, into an npn (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). The process involved two separate MBE growths, leading to base contact regions that were self-aligned to the emitter mesas. The devices could be easily probed with pressure contacts even prior to any metallization, and excellent characteristics were obtained after final metallization. Contact resistivities of 5×10^{-7} Ωcm^2 and $3 \times 10^{-6} \Omega cm^2$ were measured for n and p-type graded-gap ohmic contact structures, respectively.

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I Introduction

In 1981, Woodall et al. [1] proposed and demonstrated a non-alloyed graded-gap scheme for obtaining ohmic contacts to n-type GaAs, by first growing a graded transition from GaAs to InAs and then making a non-alloyed metallic contact to the InAs. The underlying idea was as follows. It is well known that at a metal-to-InAs interface the Fermi level is pinned inside the InAs conduction band [2], hence this interface by itself acts as an ideal negative-barrier ohmic contact. However, if the GaAs-to-InAs transition were not graded, it would act as a quasi-Schottky barrier with a barrier height close to the conduction band offset ΔE_C of the GaAs/InAs heterojunction, about 0.9 eV [3], and the contact would be poor overall. Sufficient grading flattens out the heterojunction barrier, and leads to an excellent ohmic contact with properties that make it an attractive alternative to the widely -used Au/Ge/Ni/Au alloyed system [4-6]. For p-type GaAs, the Ga(As,Sb) system could be similarly used, as proposed by Chang and Freeouf [7].

In the present work, we report the side-by-side incorporation of such n- and p-type graded-gap contacts as emitter and base contacts of a npn (Al,Ga)As/GaAs heterostructure bipolar transistor (HBT). Not only are the contact resistivities competitive with those of alloyed contacts, but the non-alloyed contacts are non-invasive. They are, therefore, particularly attractive for bipolar transistors, because emitter regions can be employed that are much thinner than those possible with alloyed contacts, leading to reduced emitter resistances. Also, the possibility of

alloying through the thin base region is eliminated with non-alloyed base contacts.

II Graded-gap contact growth procedure

As a preliminary to transistors, n- and p- type graded-gap contacts grown by molecular beam epitaxy (MBE) on (100)-oriented semi-insulating GaAs substrates were investigated separately. To keep the series path resistance of the graded region low, the doping in the graded region should be as high as possible and the graded region should be as narrow as possible, limited only by the requirement to flatten the quasi-Schottky barrier mentioned in the introduction. Theoretical investigations [8] show that graded regions as narrow as 30nm should be permissible. For the n-type graded gap contact structures, approximately 200nm of 1 x 10^{18} cm^{-3} (Si - doped) n^+-GaAs was grown at 600°C, followed by approximately 30nm of n^+-(Ga,In)As compositionally graded from GaAs to InAs. The grading was achieved by ramping the temperatures of the Ga and In furnaces. In addition, during the growth of the graded region the substrate temperature was ramped down from 600°C to 500°C because the temperature of congruent sublimation for (Ga,In)As decreases with increasing indium fraction [9]. Approximately 30nm of n^+-InAs was grown above the graded region. The doping level in the graded region and the InAs was about 3 x 10^{18} cm^{-3} .

For the p-type graded-gap contact structures a 200 nm p^+-GaAs buffer layer was grown first, followed by 30nm p^+-Ga(As,Sb), compositionally graded from GaAs to GaSb. The growth of the graded region was initiated by opening the shutter of the Sb

source. Both the antimony-to-gallium and the initial arsenic-to-gallium atomic flux ratios were approximately 3 : 1. In the presence of such an arsenic flux at a substrate temperature of 600°C, very little (< 1%) antimony gets incorporated into the growing material [10]. During the growth of the graded region the substrate temperature was then ramped from 600°C to 470°C, for two reasons. (a) The temperature of congruent sublimation of GaSb is approximately 455°C [9] which is much lower than that of GaAs. Consequently GaSb requires a lower growth temperature than GaAs. (b) The substitution of arsenic by antimony is enhanced at lower growth temperatures [10], thus facilitating the growth of the graded layer. In addition, to accomplish a complete transition to GaSb, the power to the arsenic furnace was turned off 3 min into the growth of the graded region. The arsenic flux dropped to a tenth of its initial value at the end of the growth of the graded region, while the antimony flux remained constant. About 30nm of p^+-GaSb was grown above the graded layer. The p^+-layers were doped with Be to about 5×10^{18} cm^{-3}.

III Contact resistivity measurements

The specific contact resitivities of the n and p-type graded-gap contacts were measured with a 4-point Kelvin cross resistor structure [11]. For non-alloyed (Ga,In)As graded-gap contacts to n-GaAs, contact resistivities down to 5×10^{-7} Ωcm^2 were obtained. For p-type Ga(As,Sb) graded-gap contacts resistivities down to 3×10^{-6} Ωcm^2 were measured. However, the Kelvin measurement technique is extremely sensitive to misalignment between the mesa and the ohmic metal [12]. In general, the

measurement overestimates of the contact resistivity and it is this pessimistic upper limit that is reported here. The true value of the resistivity could be much lower than the measured value.

For comparison, the typical values for Au/Ge/Ni n-type and Au/Zn p-type alloyed contacts found in the literature are 1 x $10^{-6}\Omega cm^2$ [5] and 7 x$10^{-6}\Omega cm^2$ [13]. It can be seen that our measured values are competitive with the typical values reported in the literature.

IV Transistors

The HBT structure was grown by molecular beam epitaxy on a (100) oriented n^+-GaAs substrate. The doping levels, compositions and thicknesses of the initial HBT layers are shown in Fig. 1. The region between the base and the emitter was digitally graded with a narrow-well (Al,Ga)As/GaAs superlattice [14]. The Al mole fraction in the (Al,Ga)As emitter was 0.25. The GaAs was grown at 600°C, and the (Al,Ga)As at 650°C, with arsenic to group-III atomic flux ratios of approximately 2 : 1. The growth temperature was reduced to 600°C at the end of the emitter layer, and 30nm of (Al,Ga,In)As compositionally graded from (Al,Ga)As to InAs was grown, followed by 30nm of InAs, using a procedure similar to the one described for the growth of the (Ga,In)As graded-gap contact in Section II. The graded region and the InAs were heavily doped n-type with Si to about 3 x $10^{18}cm^{-3}$.

The sample was then removed from the MBE system and SiO_2 was deposited using plasma-enhanced chemical vapor deposition (PCVD) at 300°C. The SiO_2 was patterned into the emitter mesa regions using standard photoresist techniques. The SiO_2 was used as a mask for etching the emitter mesas, with $H_3PO_4 : H_2O_2 : H_2O = 4 : 1 : 50$. The sample was then rinsed in solvents, rinsed in de-ionized water for 10 min and reloaded into the MBE system for the base contact regrowth.

The oxide was desorbed at approximately 620°C in an arsenic ambient. A small carbon peak was detected by Auger electron spectroscopy after the oxide desorption. Approximately 100nm of p^+-GaAs was grown to smooth out the restart interface. Then 30nm of p^+-Ga(As,Sb) compositionally graded from GaAs to GaSb was grown, followed by 30nm of p^+-GaSb, as described in Section II. The doping in the p^+-layers was about 5×10^{18} cm^{-3}. Because of the undercut due to the emitter mesa etch, the MBE regrowth of the p-type contacts leads to base contact regions that are self-aligned with respect to the emitter mesas, a very desirable feature.

One of the potential advantages of graded-gap contacts is that they are capable of withstanding high-temperature processing. Our growth procedure showed that the (Ga,In)As capped with SiO_2 could clearly withstand high temperatures of 620°C during the regrowth of the p-type graded-gap contact.

After the sample was removed from the MBE system the material grown on top of the SiO_2 was found to be polycrystalline. Furthermore, it appeared to be penetrated by an HF etch : the SiO_2 was easily etched off with HF, along with the material on top of the SiO_2. Base mesas were then etched, first using HF : H_2O_2 : H_2O = 10 : 1 : 100 to etch the Ga(As,Sb) and then using the phosphoric acid-based etch mentioned above to etch the GaAs. At this point the device I/V characteristics could be obtained even prior to any final metallization, using tungsten probe tips to directly contact the semiconductor surfaces of the base and the emitter. Indium alloyed on the backside of the n^+-wafer formed the collector contact. Examples of I/V curves obtained in this manner are shown in Fig. 2(a).

Finally, a dielectric (SiO_2) was deposited by PCVD, contact windows were cut and Cr/Au metallization was deposited by evaporation. Both the base and the emitter metallization were done in one step. No alloying was done. The device I/V curves obtained after final metallization is shown in Fig. 2(b). It should be noted that the I/V curves in Fig. 2(b) were obtained on devices fabricated in a different run than those corresponding to Fig. 2(a). The I/V curves were very similar to those obtained on conventional alloyed contact transistors which were fabricated in a different run.

VI Acknowledgements

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List of Figures

Fig. 1

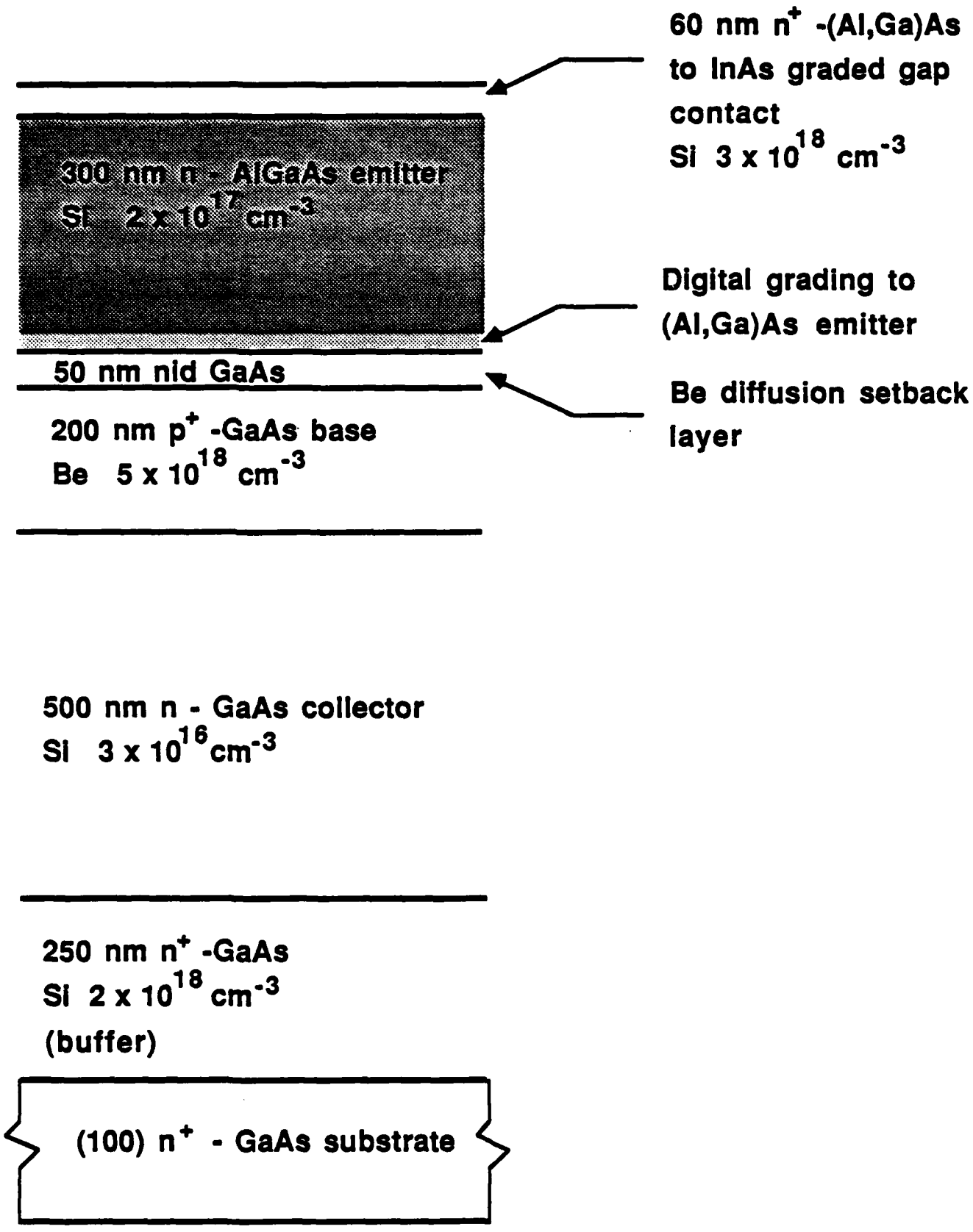
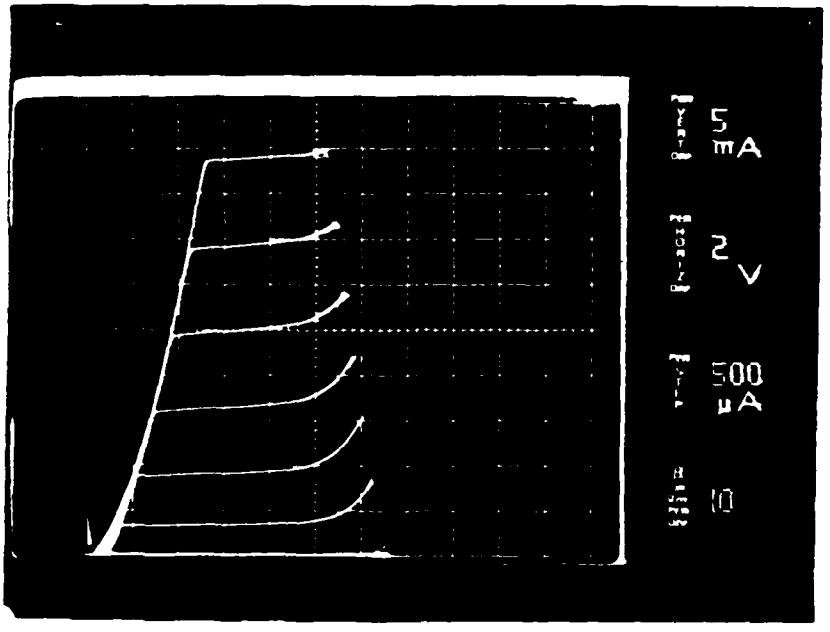
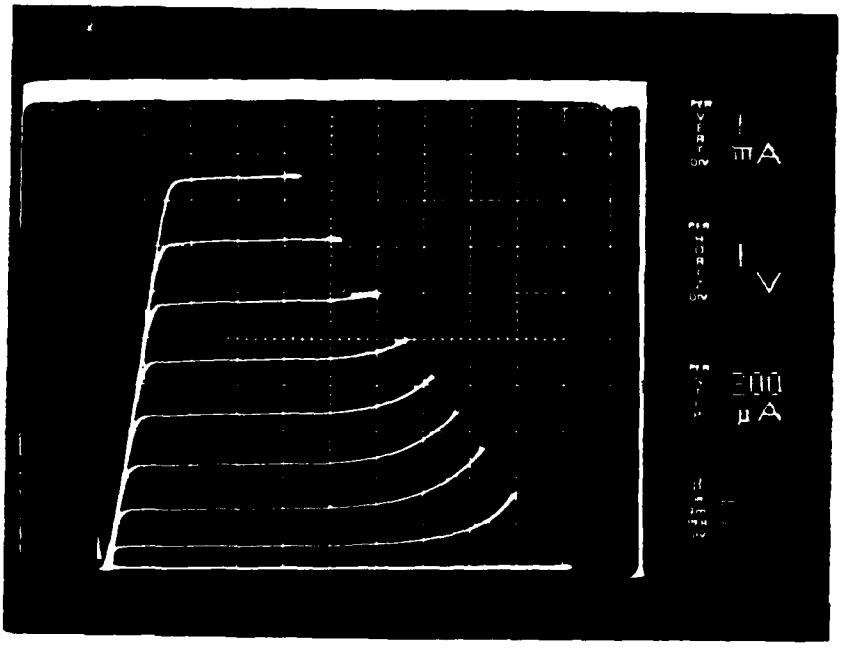

60 nm n+ -(Al,Ga)As
to InAs graded gap
contact
Si 3 x 10^18 cm^-3
300 nm n - AlGaAs emitter
Si 2 x 10^17 cm^-3
Digital grading to
(Al,Ga)As emitter
50 nm nid GaAs
Be diffusion setback
layer
200 nm p+ -GaAs base
Be 5 x 10^18 cm^-3
500 nm n - GaAs collector
Si 3 x 10^16 cm^-3
250 nm n+ -GaAs
Si 2 x 10^18 cm^-3
(buffer)
(100) n+ - GaAs substrate

Fig. 2



(a) Emitter area is 150µm x 150µm



(b) Emitter area is 20µm x 20µm

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